Product Specification

PE94302

50 Ω RF Digital Step Attenuator
For Rad-Hard Space Applications
6-bit, 31.5 dB, DC – 4.0 GHz

Features

- Attenuation: 0.5 dB steps to 31.5 dB
- Flexible parallel and serial programming interfaces
- 100 Krads (Si) Total Dose
- Positive CMOS control logic
- High attenuation accuracy and linearity over temperature and frequency
- Low power - 100 µA at 3.0V
- 50 Ω impedance

Product Description

The PE94302 is a high linearity, 6-bit UltraCMOS™ RF Digital Step Attenuator (DSA). This 50-ohm RF DSA covers a 31.5 dB attenuation range in 0.5 dB steps. It provides both parallel and serial CMOS control interface. The PE94302 maintains high attenuation accuracy over frequency and temperature and exhibits very low insertion loss and power consumption.

The PE94302 is optimized for commercial space applications. Single Event Latch up (SEL) is physically impossible and Single Event Upset (SEU) is better than 10-9 errors per bit / day. Fabricated in Peregrine's UltraCMOS™ technology, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, the PE94302 offers excellent RF performance and intrinsic radiation tolerance.

Figure 1. Functional Schematic Diagram

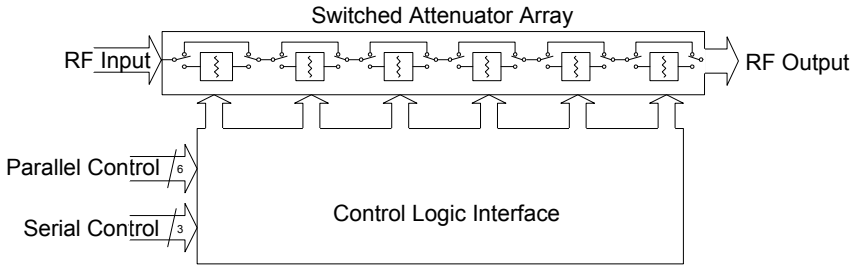


Figure 2. Package Type
28-lead CQFP

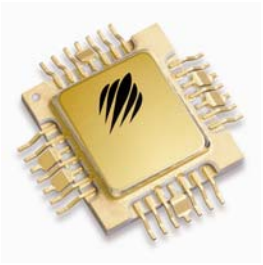


Table 1. Electrical Specifications @ -40°C ≤ Temp ≤ +85°C, 2.7V ≤ V_{DD} ≤ 3.30V

Parameter	Test Conditions	Frequency	Min	Typical	Max	Units
Operation Frequency		DC - 4000				MHz
Insertion Loss		DC - 2.2 GHz		1.5	2.75	dB
Attenuation Accuracy	0.5 dB - 8.0 dB Atten.	DC - 1.0 GHz	- (0.55 + 3.7% of atten. setting)		+ (0.55 + 3.7% of atten. setting)	dB
	8.5 dB - 31.5 dB Atten.				+ 0.9	
	0.5 dB - 4.0 dB Atten.	1.0 - 2.2 GHz			+ (0.70 + 3.0% of atten. setting)	
	4.5 dB - 31.5 dB Atten.				+ 0.9	
	0.5 dB - 23.0 dB Atten.		- (0.7+ 3.0% of atten. setting)			
	23.5 dB - 31.5 dB Atten.		- (0.6 + 9.0% of atten. setting)			
1 dB Compression		1 MHz - 2.2 GHz		33		dBm
Input IP3	Two-tone inputs			52		dBm
Return Loss		DC - 2.2 GHz		15		dB
RF Input Power (50 Ω)					12	dBm
Switching Speed	Min to Max Atten. State			1		µs

Notes: 1. Device Linearity will begin to degrade below 1 MHz
2. Maximum Operating Power = +12 dBm
3. Specs are guaranteed to 2.2 GHz, Characterized to 4.0 GHz

Figure 3. Pin Configuration (Top View)

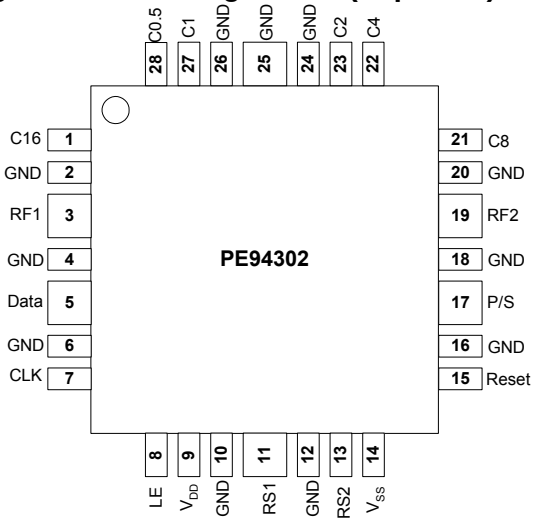


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	C16	Attenuation control bit, 16dB
2	GND	Ground connection
3	RF1	RF port (Note 1).
4	GND	Ground connection
5	Data	Serial interface data input
6	GND	Ground connection
7	CLK	Serial interface clock input.
8	LE	Latch Enable input (Note 2).
9	V_{DD}	Power supply pin.
10	GND	Ground connection
11	RS1	Redundant Signal (note 3)
12	GND	Ground connection
13	RS2	Redundant Signal (Note 3)
14	V_{SS}	Negative supply voltage (Note 4)
15	Reset	Reset (Note 5)
16	GND	Ground connection
17	P/S	Parallel/Serial mode select.
18	GND	Ground connection
19	RF2	RF port (Note 1).
20	GND	Ground connection
21	C8	Attenuation control bit, 8 dB.
22	C4	Attenuation control bit, 4 dB.
23	C2	Attenuation control bit, 2 dB.
24	GND	Ground connection
25	GND	Ground connection
26	GND	Ground connection
27	C1	Attenuation control bit, 1 dB.
28	C0.5	Attenuation control bit, 0.5 dB.
Paddle	GND	Ground connection

Note 1: Both RF ports must be held at 0 V_{DC} or DC blocked with an external series capacitor.
2: Latch Enable (LE) has an internal 100 kΩresistor to $V_{DD.}$
3: Must be tied to Vdd or GND under normal operation.
4: Must be tied to external supply with V_{SS} = -V_{DD}
5: Must be tied to GND under normal operation

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Power supply voltage	-0.3	4.0	V
V_{ss}	Negative Power supply voltage (-V_{DD})	-4.0	0.3	V
V_I	Voltage on any DC input	-0.3	V_{DD}+ 0.3	V
T_{ST}	Storage temperature range	-65	150	°C
P_{IN}	Input power (50Ω)		24	dBm
V_{ESD}	ESD voltage (Human Body Model)		500	V

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Table 4. Operating Ranges

Parameter	Min	Typ	Max	Units
V_{DD} Power Supply Voltage	2.7	3.0	3.3	V
V_{ss} Power Supply Voltage	-3.3	-3.0	-2.7	V
I_{DD} Power Supply Current			250	µA
I_{ss} Power Supply Current	-500			µA
T_{OP} Operating temperature range	-40		85	°C
Digital Input High	0.7xV_{DD}			V
Digital Input Low			0.3xV_{DD}	V
Digital Input Leakage			1	µA

Exposed Solder Pad Connection

The exposed solder pad on the bottom of the package must be grounded for proper device operation.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rate specified.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Switching Frequency

The PE94302 has a maximum 25 kHz switching rate.

Programming Options

Parallel/Serial Selection
Either a parallel or serial interface can be used to control the PE94302. The P/S bit provides this selection, with P/S=LOW selecting the parallel interface and P/S=HIGH selecting the serial interface.

Parallel Mode Interface
The parallel interface consists of six CMOS-compatible control lines that select the desired attenuation state, as shown in Table 5.

The parallel interface timing requirements are defined by Figure 5 (Parallel Interface Timing Diagram), Table 8 (Parallel Interface AC Characteristics), and switching speed (Table 1).

For *latched* parallel programming the Latch Enable (LE) should be held LOW while changing attenuation state control values, then pulse LE HIGH to LOW (per Figure 5) to latch new attenuation state into device.

For *direct* parallel programming, the Latch Enable (LE) should be either pulled high or floated (see Table 2, note 2). Changing attenuation state control values will change device state to new attenuation. Direct Mode is ideal for manual control of the device (using hardwire, switches, or jumpers).

Table 5. Truth Table

P/S	C16	C8	C4	C2	C1	C0.5	Attenuation State
0	0	0	0	0	0	0	Reference Loss
0	0	0	0	0	0	1	0.5 dB
0	0	0	0	0	1	0	1 dB
0	0	0	0	1	0	0	2 dB
0	0	0	1	0	0	0	4 dB
0	0	1	0	0	0	0	8 dB
0	1	0	0	0	0	0	16 dB
0	1	1	1	1	1	1	31.5 dB

Note: Not all 64 possible combinations of C0.5-C16 are shown in table

Serial Interface
The serial interface is a 6-bit serial-in, parallel-out shift register buffered by a transparent latch. It is controlled by three CMOS-compatible signals: Data, Clock, and Latch Enable (LE). The Data and Clock inputs allow data to be serially entered into the shift register, a process that is independent of the state of the LE input.

The LE input controls the latch. When LE is HIGH, the latch is transparent and the contents of the serial shift register control the attenuator. When LE is brought LOW, data in the shift register is latched.

The shift register should be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data. The timing for this operation is defined by Figure 4 (Serial Interface Timing Diagram) and Table 7 (Serial Interface AC Characteristics).

Figure 4. Serial Interface Timing Diagram

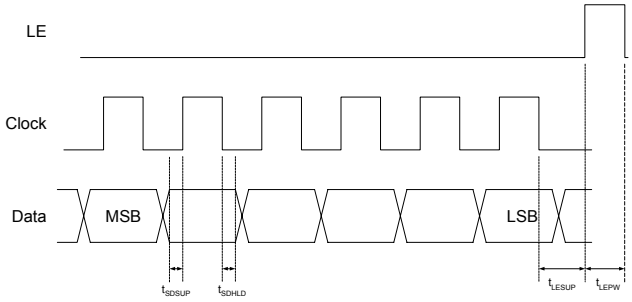


Table 6. 6-Bit Attenuator Serial Programming Register Map

B5	B4	B3	B2	B1	B0
C16	C8	C4	C2	C1	C0.5

MSB (first in) LSB (last in)

Figure 5. Parallel Interface Timing Diagram

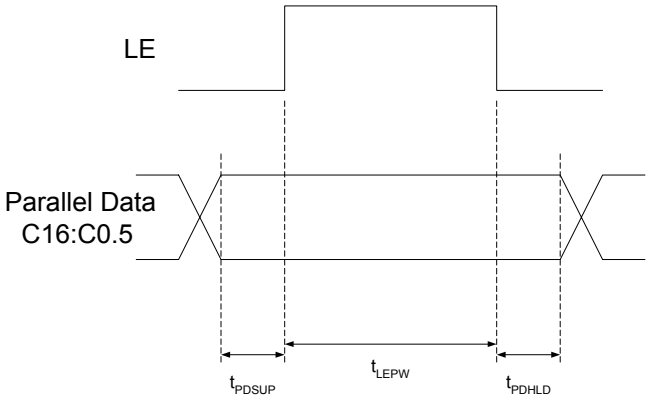


Table 7. Serial Interface AC Characteristics

V_{DD} = 3.0 V, -40° C < T_A < 85° C, unless otherwise specified

Symbol	Parameter	Min	Max	Unit
f_{Clk}	Serial data clock frequency (Note 1)		10	MHz
t_{ClkH}	Serial clock HIGH time	30		ns
t_{ClkL}	Serial clock LOW time	30		ns
t_{LESUP}	LE set-up time after last clock falling edge	10		ns
t_{LEPW}	LE minimum pulse width	30		ns
t_{SDSUP}	Serial data set-up time before clock rising edge	10		ns
t_{SDHLD}	Serial data hold time after clock falling edge	10		ns

Note: f_{Clk} is verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10 MHz to verify fclk specification.

Table 8. Parallel Interface AC Characteristics

V_{DD} = 3.0 V, -40° C < T_A < 85° C, unless otherwise specified

Symbol	Parameter	Min	Max	Unit
t_{LEPW}	LE minimum pulse width	10		ns
t_{PDSUP}	Data set-up time before rising edge of LE	10		ns
t_{PDHLD}	Data hold time after falling edge of LE	10		ns

Typical Performance Data @ 25°C, V_{DD} = 3.0 V

Figure 6. Input Return Loss vs. Frequency

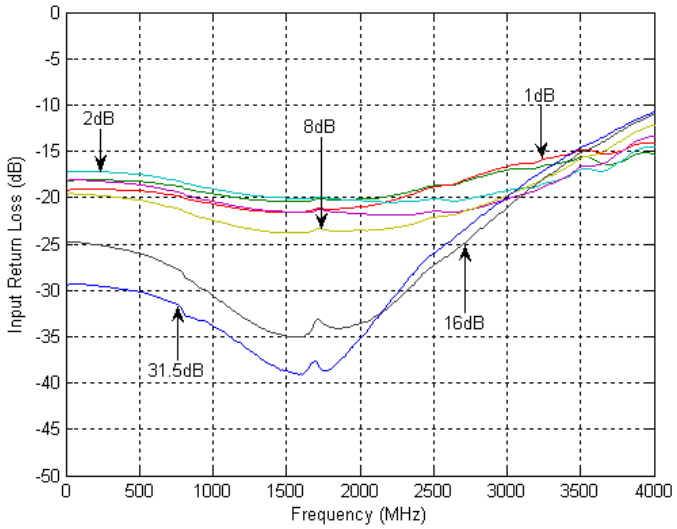


Figure 7. Output Return Loss vs. Frequency

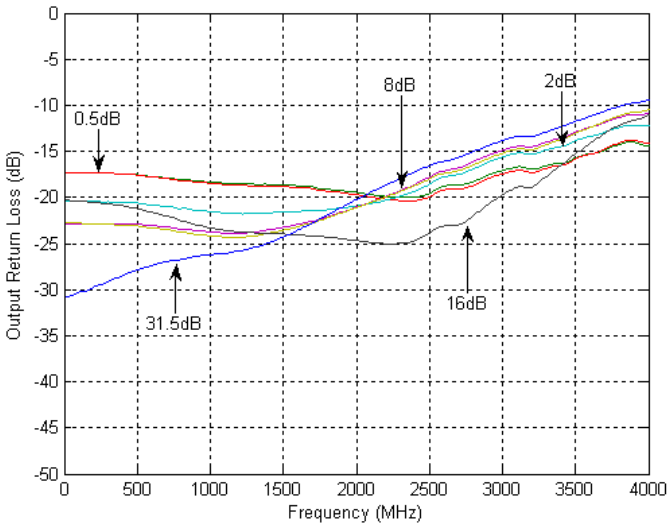


Figure 8. Insertion Loss

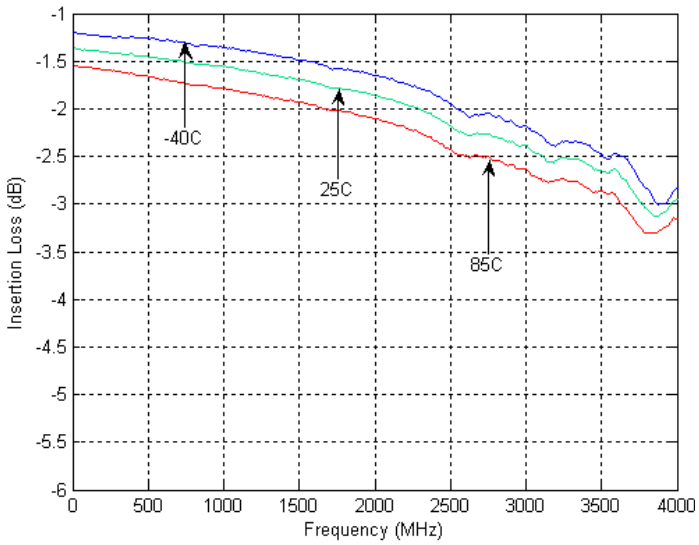
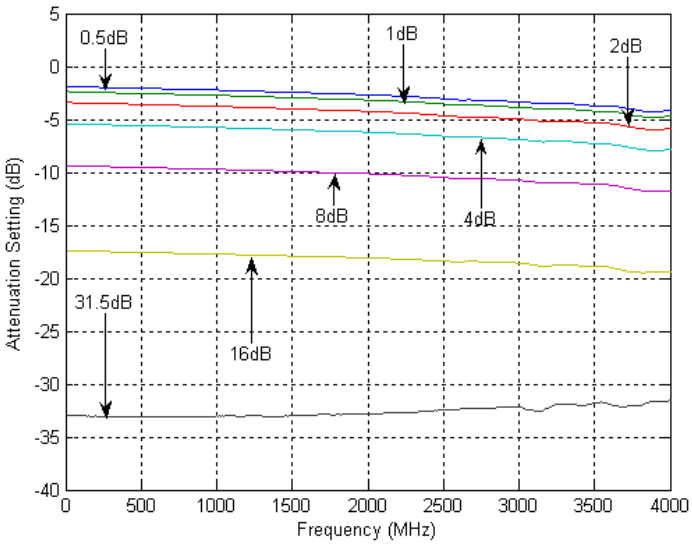


Figure 9. Attenuation Setting vs. Frequency



Typical Performance Data @ 25°C, V_{DD} = 3.0 V

Figure 10. Attenuation Error vs. Frequency

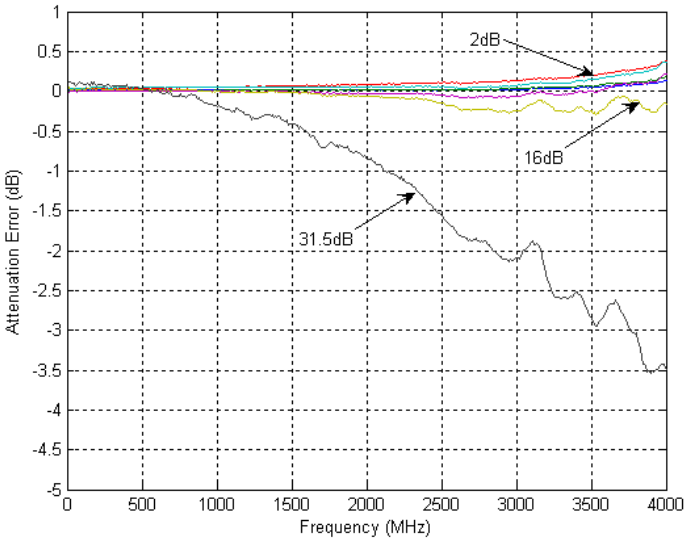


Figure 11. Attenuation Error vs. Setting

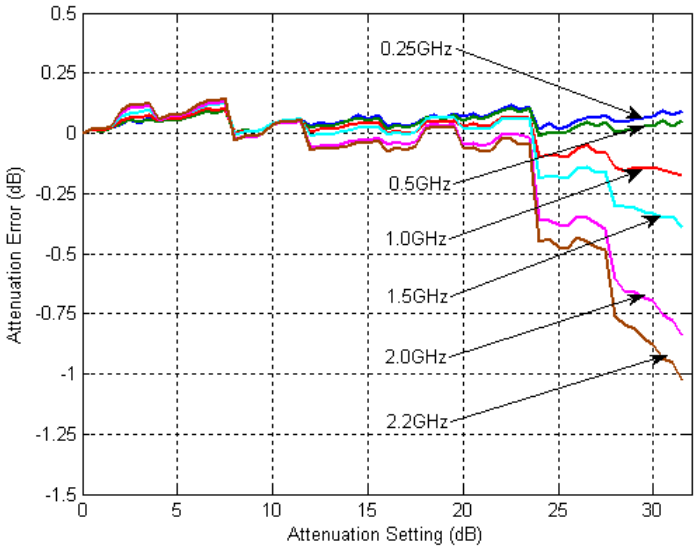


Figure 12. IIP3 vs. Frequency

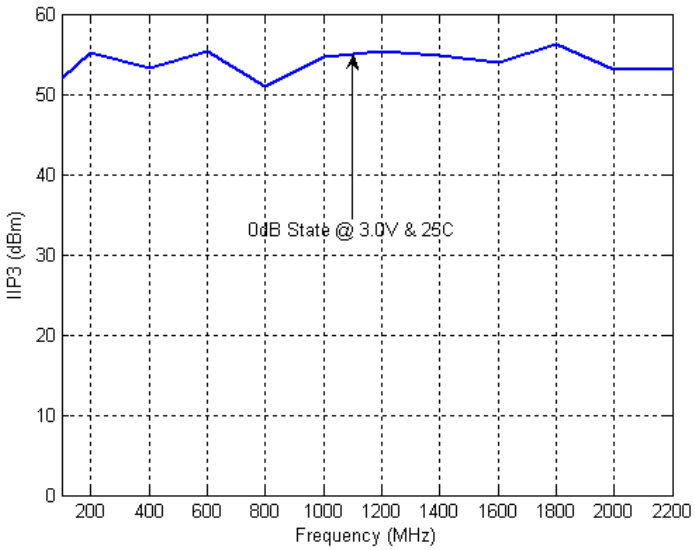


Figure 13. 1 dB Compression vs. Frequency

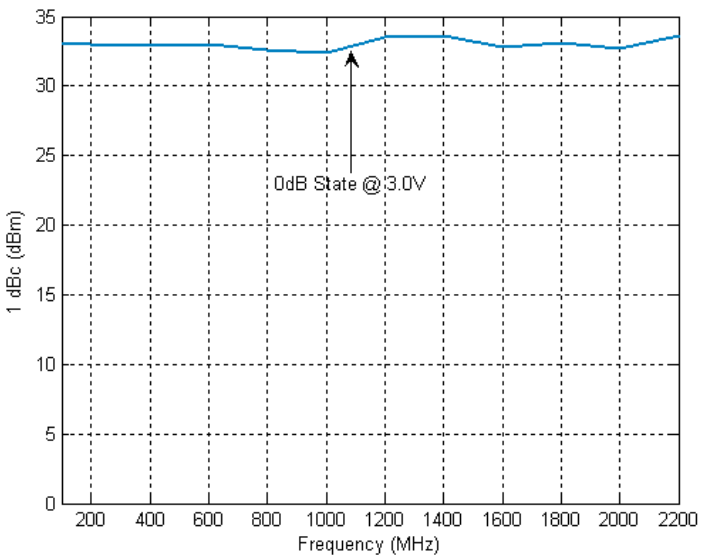
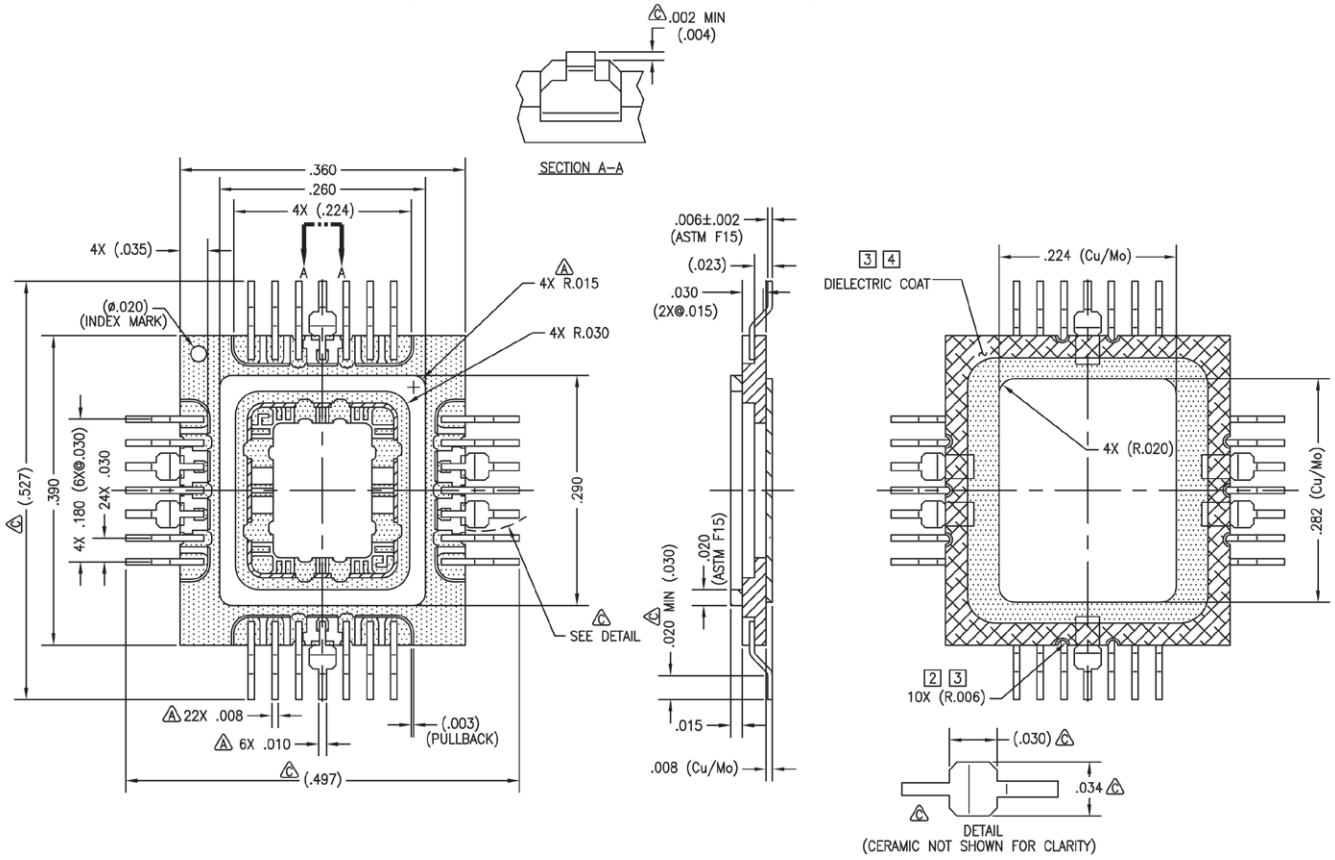


Figure 14. Package Drawing (dimensions in inches)

28-lead CQFP



NOTES:

1. METALLIZATION/PLATING: REFRACTORY METAL + Ni (75~350u") + Au (50u"MIN.).
2. METALLIZED CASTELLATIONS.
3. DIELECTRIC RUN INTO CASTELLATIONS SHALL BE ACCEPTABLE.
4. GOLD SPECKLES ON DIELECTRIC COAT SHALL BE ACCEPTABLE.
5. VISUAL ANOMALIES IN CASTELLATION METALLIZATION ACCEPTABLE.
6. TEXT AND ITS LOCATIONS ON LEAD FRAME ARE VENDOR'S OPTION.
7. SLIGHT PATTERN MISMATCH WITH DRAWING DUE TO DIELECTRIC COAT MISALIGNMENT SHALL BE ACCEPTABLE.
8. SEAL RING & HEAT SINK ARE CONNECTED TO GND.
9. LEAD INTEGRITY(ADHESION/ALIGNMENT/COPRANARITY), CASTELLATION QUALITY ARE BEST EFFORT BASIS.

Table 9. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
94302-01	94302	PE94302-28CQFP-50B Engineering Samples	28-lead CQFP	25 Count Trays
94302-11	94302	PE94302-28CQFP-50B Production Units	28-lead CQFP	25 Count Trays
94302-00	PE94302-EK	PE94302 Evaluation Kit	Evaluation Board	1 / Box

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Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a DCN (Document Change Notice).

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